IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Patent Application of)	Examiner: Verbrugge, K.
)	
Thomas J. Holman)	Art Unit: 2751
)	
Serial No. 09/023,172)	
)	
Filed: February 13, 1998)	
)	
For: MEMORY MODULE CONTROLLER)	
FOR PROVIDING AN INTERFACE)	
BETWEEN A SYSTEM MEMORY)	
CONTROLLER AND A PLURALITY)	
OF MEMORY DEVICES ON A)	
MEMORY MODULE (As Amended))	

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Signature   Date

HONORABLE COMMISSIONER OF
PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPEAL BRIEF
(Under 35 C.F.R. § 1.192)

Sir:

This is an appeal to the Board of Patent Appeals and Interferences from the

decision of the Examiner of Group 2751, dated July 3, 2000, who finally rejected claims

1-14 in the above-identified application. This Appeal Brief is filed under 37 C.F.R. §

1.192. This Appeal Brief is submitted in triplicate pursuant to 37 C.F.R. § 1.192(a).

I.   REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052.

II.   RELATED APPEALS AND INTERFERENCES

Appellant identifies the following related applications, which may directly affect, be directly affected by, or have a bearing on the Board's decisions in connection with the present application.

The present application is related to and claims the benefit of U.S. Provisional Application No. 60/067,824, entitled "DISTRIBUTED CONTROL MEMORY BUS ARCHITECTURE," filed on December 5, 1997 and U.S. Provisional Application No. 60/067,588, entitled "DISTRIBUTED CONTROL MEMORY BUS ARCHITECTURE," also filed on December 5, 1997.

The above-identified application is also related to co-pending U.S. Patent Application No. 09/023,170 ('170 Application), entitled "MEMORY SYSTEM INCLUDING A MEMORY MODULE HAVING A MEMORY MODULE CONTROLLER,"[1] filed on February 13, 1998 and U.S. Patent Application No. 09/023,234 ('234 Application), entitled "MEMORY MODULE INCLUDING A MEMORY MODULE CONTROLLER,"[2] filed on February 13, 1998. A Notice of Appeal was filed on October 23, 2000 for the '170 Application. A Notice of Appeal was filed on September 27, 2000 for the '234 Application.

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[1]   The title of the '170 Application has been amended to "MEMORY SYSTEM INCLUDING A MEMORY MODULE HAVING A MEMORY MODULE CONTROLLER INTERFACING BETWEEN A SYSTEM MEMORY CONTROLLER AND MEMORY DEVICES ON THE MEMORY MODULE."
[2]   The title of the '234 Application has been amended to "MEMORY MODULE HAVING A MEMORY MODULE CONTROLLER CONTROLLING MEMORY TRANSACTIONS FOR A PLURALITY OF MEMORY DEVICES."

The aforementioned provisional and co-pending applications are assigned to the same assignee of the present application on appeal.

III.   STATUS OF THE CLAIMS

Claims 1-14 are finally rejected. Claims 1-14 are the subject of this appeal.

Claims 1-14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy *et al.* ("Levy").

Claims 3, 4, and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Levy.

Claims 1-14 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of co-pending Application No. 09/023,170 ('170 Application) and claims 1-17 co-pending Application No. claims 09/023,234 ('234 Application).

A copy of claims 1-14 as they stand on appeal are set forth in the attached Appendix.

IV.   STATUS OF AMENDMENTS

The present application was filed on February 13, 1998 with claims 1 through 14.

In the Office Action mailed February 9, 1999, the Examiner rejected claims 1-14 under 35 U.S.C. § 103(a) as being unpatentable over "Memory Systems Design and Applications," edited by Dave Bursky, pp. 213-220 (Bursky Reference) and rejected claims 1-14 under 35 U.S.C. § 101 double patenting rejection as conflicting with claims 1-20 of the '170 Application and claims 1-17 of the '234 Application.

In response to the February 9, 1999 Office Action, Appellant filed a Continued Prosecution Application on August 9, 1999.

In the Office Action mailed on September 13, 1999, the Examiner provided new grounds of rejection in which claims 1-14 were rejected under 35 U.S.C. 102(b) as being anticipated by the Bursky Reference. The Examiner also provisionally rejected claims 1-14 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of the '170 Application and claims 1-17 over the '234 Application.

In response to the September 13, 1999 Office Action, Appellant filed an amendment on March 2, 2000. In the March 2, 2000 amendment, Appellant amended claims 1-14 and requested allowance of claims 1-14 over the Bursky Reference. Appellant also stated that upon a condition of allowance of one or more claims, Appellant will submit a timely terminal disclaimer to overcome the provisional double patenting rejection of claims 1-14 of the present application.

In the Office Action mailed on July 3, 2000, the Examiner provided a Final Rejection based on newly cited prior art. More particularly, the Examiner rejected claims 1, 2, and 6-14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,045,781 to Levy et al. ("Levy") and claims 3, 4, and 5 under 35 U.S.C. § 103(a) as being unpatentable over Levy. The Examiner maintained the previous provisional double-patenting rejection of claims 1-14 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of the '170 Application and claims 1-17 over the '234 Application.

In response to the July 3, 2000 Final Office Action, Appellant filed an Amendment After Final on August 24, 2000. In the August 24, 2000 Amendment After Final, Appellant amended claims 1-2, 4-11, and 13-14 and requested allowance of claims 1-14 over Levy. Appellant again stated that upon a condition of allowance of one or

more claims, Appellant will submit a timely terminal disclaimer to overcome the provisional double patenting rejection of claims 1-14 of the present application.

In the Advisory Action mailed on September 7, 2000, the Examiner stated that the proposed amendments contained in the August 24, 2000 After Final Amendment will be entered upon filing a Notice of Appeal and an Appeal Brief.

In response to the September 7, 2000 Advisory Action, Appellant filed the Notice of Appeal on September 27, 2000 and this subsequent Appeal Brief. Accordingly, the amendments in the August 24, 2000 After Final Amendment are entered for purposes of appeal.

V.   SUMMARY OF THE INVENTION

The present invention is defined by claims 1-14 and their equivalents. This section of the Appeal Brief is set forth merely to comply with the requirements of 37 C.F.R. § 1.192(c)(5) and is not intended to limit claims 1-14 or its equivalents in any way. *See* M.P.E.P. 1206.

Claim 1 describes a memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module. The memory module controller includes a first interface circuitry to receive from the system memory controller a first memory transaction in a first format and a control logic coupled to the first interface circuitry and to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices. The second format of the second memory transaction is different from the first format of the first memory transaction.

The specification and drawings set forth embodiments of the invention, as defined, e.g., in claim 1. **FIG. 3** shows memory module controllers 310 and 316 coupled with a system memory controller 304 via system memory bus 323. Memory module controller 310 is coupled to a plurality of memory devices 312 through 315 via local memory module busses 330, 332, and 334-337. Memory module controller 316 is coupled to a plurality of memory devices 317-320 via local memory module busses 338, 340, and 341-344. (Spec. pp. 10-12). Memory module controllers 310 operate as bridges between system memory bus 323, that operates in one protocol or format, and local or memory module busses (e.g., lines 330, 332, and 334-337) that operate in a second different protocol format. (Spec. p.12, lines 19-22).

Thus, memory module controllers 310 and 316 for each memory module is an interface between system memory controller 304 and individual memory devices (e.g., memory devices 312-315 and 316-320) on the modules 306 and 308. Such an architecture allows for decoupling of individual memory devices form the system memory bus 323 and the system memory controller 304. This allows for the independent development of the memory device technology. For example, the memory devices may be developed to be faster, wider, to operate at different operating supply voltages, or to operate with reduced voltage swings than if the memory devices where directly communicating with the system memory controller. (Spec. p. 9, lines 14-23).

VI. ISSUES

I. Whether claims 1, 2, and 6-14 are anticipated under 35 U.S.C. §

102(b) over Levy.

II. Whether claims 3, 4, and 5 are unpatentable under 35 U.S.C. §

103(a) over Levy.

VII. GROUPING OF CLAIMS

With regards to the grounds of rejection related to issues I and II, claims 1-14

stand or fall together. Claim 1 is the representative claim for groups I and II.

VIII. ARGUMENTS

A. Levy Fails to Anticipate Claim 1 Under 35 U.S.C. § 102(b) By Failing to Disclose Each and Every Limitation of Claim 1

Appellant respectfully disagrees with the Examiner's rejection of claims 1-14

under 35 U.S.C. § 102(b) with respect to Levy. In particular, the Examiner has stated

that:

> Regarding claims 1, 12, and 13, Levy shows a memory module 30 which includes a memory module controller and a plurality of memory devices (low stack 0-3 and high stack 0-3) in Fig. 1.
> Levy shows the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42 and their input and output lines. Levy shows the claimed first interface circuitry (input lines into memory transceiver 41 and memory control and timing unit 42) which receives a first memory transaction from a system memory controller (memory management unit 22) in a first format as claimed.
> Levy further shows the claimed control logic (memory transceiver 41 and memory control and timing unit 42) which is coupled to the first memory transaction in a second format for the plurality of memory devices as claimed. The second memory format is clearly different from the first memory transaction since the outputs of the memory transceiver 41 and

.memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures and disclosure.

(p. 4 Final Office Action 7/3/00).

Appellant respectfully submits that claim 1 on appeal is not anticipated by Levy.

To anticipate claim 1, Levy must disclose each and every limitation of claim 1. Claim 1

includes the limitations of:

> 1.   A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:
> first interface circuitry to receive from the system memory controller <u>a first memory transaction in a first format</u>; and
> >   control logic coupled to the first interface circuitry and <u>to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction</u>.

(Claim 1)(emphasis added).

Levy, however, fails to disclose a memory module controller having a first

interface circuitry and a control logic coupled to the first interface circuitry in which the

control logic is to <u>convert the first memory transaction into a second memory transaction</u>

<u>in a second format for the plurality of memory devices</u> as recited in claim 1. Levy

further fails to disclose that the <u>second format of the second memory transaction is</u>

<u>different from the first format of the first memory transaction</u> as recited in claim 1.

Levy, in Figure 1, discloses a memory module 30 coupled to associative memory

24. Memory module 30 includes a memory transceiver 41 and memory control and

timing circuit 42 coupled to low and high stacks 44 and 45, respectively. The Examiner associates memory transceiver 41 and memory control and timing circuit 42 of Levy with the claimed memory module controller as recited in claim 1.

The memory transceiver 41 and memory control and timing 42, however, are not related to converting a memory transaction in a first format into a memory transaction in a second format. In particular, Levy discloses that:

> . . . During a writing operation, the associative memory 24 transmits BYTE MASK signals (FIG. 5) to the memory control and timing circuit 42 thereby to select one byte or some combination of bytes in the addressed location.
> Still referring to FIGS. 1 and 5, the associative memory 24 transmits an ADDRESS PARITY signal which is based upon the value of the address and various control signals that initiate a memory cycle and also data signals if data is being transferred from the associative memory 24. Next the associative memory 24 transmits a START signal that enables the memory control and timing circuit 42 (FIG. 1) to initiate a memory cycle. The circuit 42 transmits back to the associative memory 24 an ACKNOWLEDGE signal that terminates the address and control signals and the BYTE MASK, parity, data and START signals. During a reading memory cycle, the associative memory 24 can initiate another memory cycle with another memory until after the ACKNOWLEDGE signal is terminated.

Thus, Levy teaches that memory control and timing circuit 42 initiates a memory cycle after receiving BYTE MASK and ADDRESS PARITY signals. As such, the memory and control timing circuit of 42 of Levy does not teach converting a first memory transaction into a second memory transaction as recited in claim 1. Furthermore, nowhere in Levy does it disclose converting a first memory transaction into a second

memory transaction and <u>that the second memory transaction is different than the first memory transaction</u> as recited in claim 1.

Therefore, for the above reasons, claim 1 is not anticipated by Levy under 35 U.S.C. § 102(b) and is patentable over Levy because Levy does not disclose each and every limitation of claim 1.

B.   Claim 1 is Patentable Over Levy Under 35 U.S.C. § 103(a) Because Levy Does Not Disclose or Suggest Each and Every Limitation of Claim 1

Appellant respectfully submits that claim 1 on appeal is not obvious under 35 U.S.C. § 103(a) over Levy. For claim 1 to be rendered obvious by Levy, Levy must disclose or suggest each and every limitation of claim 1. Furthermore, the Examiner cannot rely on impermissible hindsight of the Appellant's disclosure.

In contrast to claim 1, Levy fails to disclose or suggest a memory module controller having a first interface circuitry and a control logic coupled to the first interface circuitry in which the control logic is to <u>convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices</u> as recited in claim 1.

In further contrast to claim 1, Levy further fails to disclose or suggest that the <u>second format of the second memory transaction is different from the first format of the first memory transaction</u> as recited in claim 1.

As noted above, Levy discloses a memory control and timing circuit 42 to initiate a memory cycle. Nowhere in Levy does it disclose or suggest the memory control and

timing circuit 42 to <u>convert a first memory transaction into a second memory transaction</u> and that the <u>second memory transaction is different that the first memory transaction</u> as recited in claim 1.

Therefore, claim 1 is patentable over Levy under 35 U.S.C. §103(a) because Levy fails to disclose or suggest each and every limitation of claim 1.

Reviewing the claimed structure set forth in claims 1-14, the distinctions between the cited prior art and the claimed invention are readily apparent. Therefore, Appellant respectfully contends that once the Board reevaluates the applicability of the cited prior art in view of the limitations of the claims, it will be determined that the claims are clearly distinguishable over the prior art of record.

FEE FOR FILING A BRIEF IN SUPPORT OF APPEAL

Enclosed is a check in the amount of $310.00 to cover the fee for filing of a brief in support of an appeal required under 37 C.F.R. 1.17(f) and 1.192.
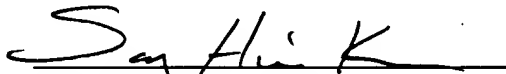
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: _Dec. 22_____, 2000

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APPENDIX

The claims on appeal read as follows:

1. A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module, comprising:

first interface circuitry to receive from the system memory controller a first memory transaction in a first format; and

control logic coupled to the first interface circuitry and to convert the first memory transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

2. The memory module controller of claim 1, further comprising:

second interface circuitry coupled to the control logic and to transmit the second memory transaction to at least one of the plurality of memory devices.

3. The memory module controller of claim 1, wherein the first memory transaction includes time multiplexed address and command information.

4. The memory module controller of claim 3, wherein the first interface circuitry comprises:

request handling logic to separate the address and command information and to provide the separate address and command information to the control logic.

5. The memory module controller of claim 4, wherein the first memory transaction further includes time multiplexed data information, and wherein the request handling logic is to separate the time multiplexed data information and to provide the separated time multiplexed data information to the control logic.

6. The memory module controller of claim 1, wherein the first interface circuitry comprises:

handshaking logic to provide a handshake signal to the system memory controller that indicates when the memory module controller is communicating data to the system memory controller.

7. The memory module controller of claim 1, wherein the first interface circuitry comprises:

data handling logic to receive data for the first memory transaction from the system memory controller and to reformat the data for the second memory transaction.

8.   The memory module controller of claim 1, further comprising:

a write buffer coupled to the first interface circuitry and to store data sent with the

first memory transaction.

9.   The memory module controller of claim 8, further comprising:

an address storage unit coupled to the write buffer and the first interface circuitry and

the address storage unit is to store addresses associated with the data stored in the write

buffer.

10.   The memory module controller of claim 1, further comprising:

a read buffer coupled to the control logic and to store data read from at least one of

the plurality of memory devices.

11.   The memory module controller of claim 1, further comprising:

a clock generator circuit coupled to the control logic and to receive a first clock signal

from the system memory controller and to generate a second clock signal for the plurality of

memory devices.

12.   A memory module controller for providing an interface between a system memory

controller and a plurality of memory devices on a memory module, comprising:

means for receiving from the system memory controller a first memory transaction in a first format; and

means for converting the first transaction into a second memory transaction in a second format for the plurality of memory devices, wherein the second format of the second memory transaction is different from the first format of the first memory transaction.

13.   A memory module controller for providing an interface between a system memory controller and a plurality of memory devices on a memory module comprising:

first interface circuitry to receive from the system memory controller a first memory transaction in a first format; and

control logic coupled to the first interface circuitry and to reformat the first memory transaction such that the plurality of memory devices perform the reformatted first memory transaction.

14.   The memory module controller of claim 13, further comprising:

second interface circuitry coupled to the control logic and to receive from one of the plurality of memory devices a second memory transaction in a second format, wherein the control logic is to reformat the second memory transaction such that the system memory controller is to perform the reformatted second memory transaction.